Garmin Power Sensor Test Fixture

DESIGN DOCUMENT

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1 Introduction

1.1 PROJECT STATEMENT

During product development at Garmin, engineers want to be able to measure the power consumed by parts of their circuits within their fitness electronics. Our power sensor fixture will have eight channels with two probes per channel capable of measuring currents from 10 uA to 10 mA and voltages from 0 to 5.5 V. We will use a microcontroller to calculate power consumption with the aforementioned measurements, and an SD card will be capable of storing the data. Garmin engineers hope to hook up our fixture to different circuit sections of a gadget and let it run overnight to obtain a comprehensive set of power consumption data points.

1.2 PURPOSE

Fitness electronics are driving a healthier society. Garmin is a leader in this market, and we are providing a tool that will allow engineers to not only work more efficiently but also to work with more information. This information allows them to make more informed design choices that will lead to a safe, useful electronic device.

1.3 GOALS

- Conduct ourselves professionally during meetings and in online correspondence

- Set realistic deadlines and meet them

- Keep costs under $300 per unit

- Submit a CADSTAR printed circuit board design by end of first semester

- Create user-friendly manual switches and settings

- Design a dummy-proof system that will prevent incorrect manual settings

- Perform useful tests that will lead to optimization in the second round of design work

- Deliver a working product to our client by May 2017

2 Deliverables

November 2016: PSPICE Circuit Simulation

November 2016: Breadboard Circuit Design

November/December 2016: Plan & Design Documentation Submittals

December 2016: CADSTAR Design sent to Garmin

January/February 2017: Test Results, Analysis, and Optimization

March 2017: Second CADSTAR Design sent to Garmin

April 2017: Final Documentation & Presentation

3 Design

Include any/all possible methods of approach to solving the problem. Discuss what you have done so far. What have you tried/implemented/tested etc. We want to know what you have done.

3.1 SYSTEM SPECIFICATIONS

The following bulleted specifications are based on requirements given by our client as well as parameters of our chosen components.

3.1.1 Non-functional

- Printed circuit board will not exceed 30 square inches

3.1.2 Functional

- Measure currents from 10 μA to 10 mA

- Measure voltages from 0 to 5.5 V

- Convert voltage range to 0 to 3.0 V before ADC

- Maximum ADC input capacitance of 5 pF

- Use microcontroller to compute power consumption with above measurements

- Replicate first channel circuit to bring channel total to 8

- Use SD card to store large amounts of data

3.2 PROPOSED DESIGN/METHOD

Figure 1 shows a high-level block diagram of the project. All parts before the ADC are shown in greater detail – including circuit components and resistor values – in Figure 2.

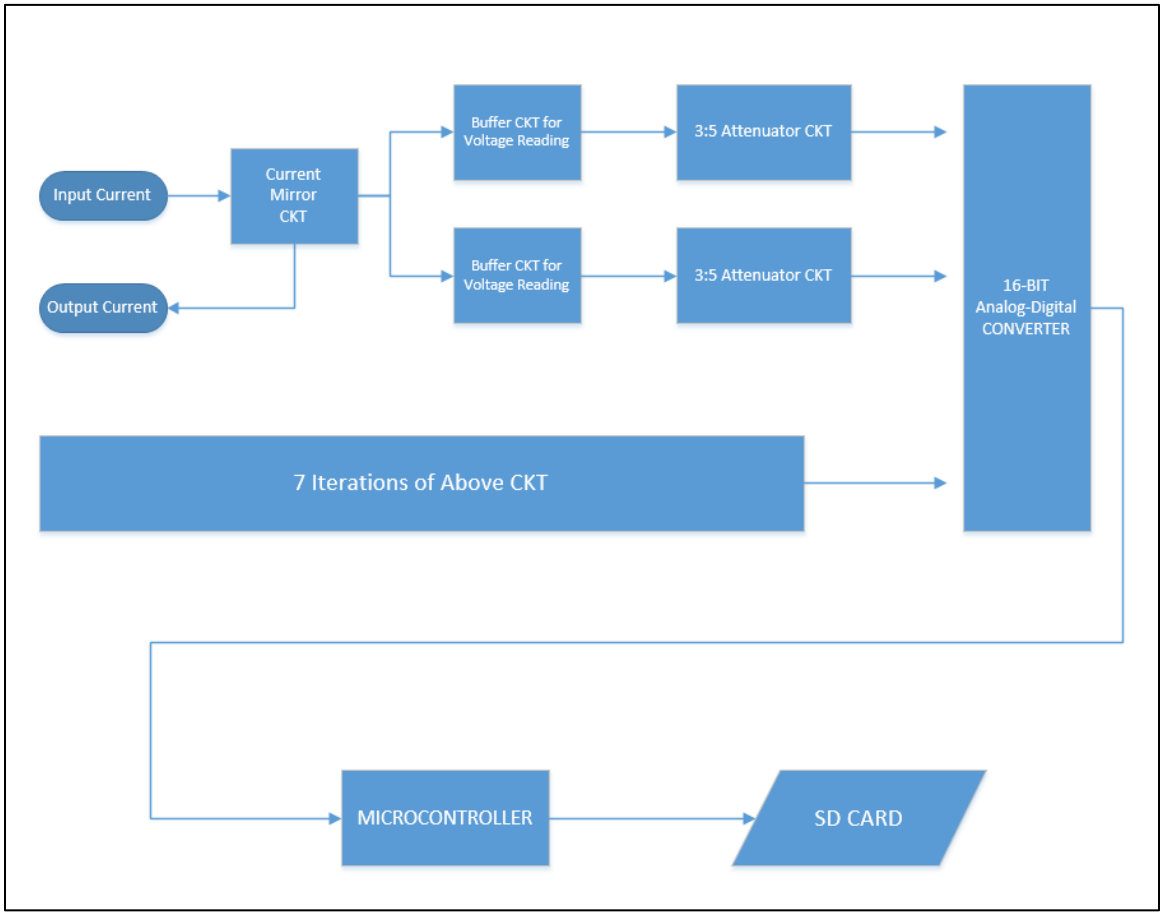


Figure 1

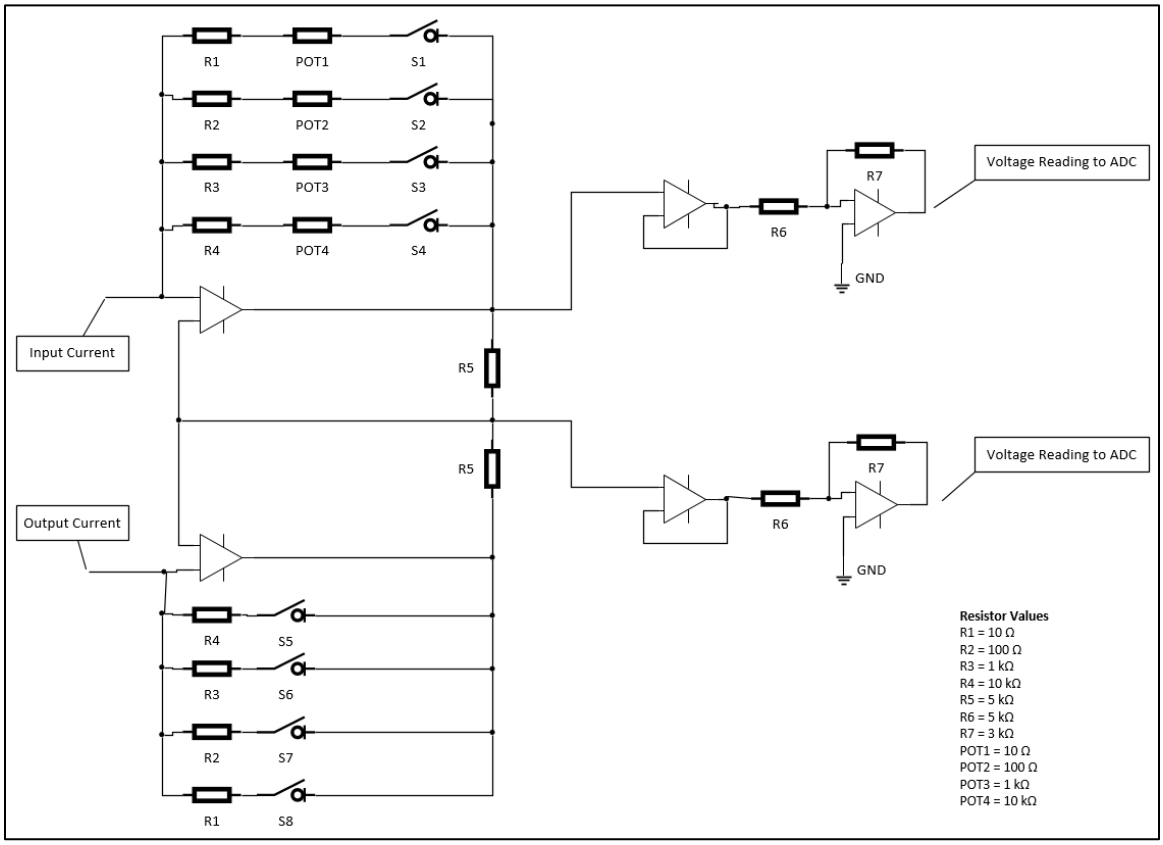

R1
POT1
S1
R2
POT2
S2
R3
POT3
S3
R4
POT4
S4
Input Current
R5
R5
Output Current
R4
S5
R3
S6
R2
S7
R1
S8
R7
R6
GND
Voltage Reading to ADC
R7
R6
GND
Voltage Reading to ADC
Resistor Values
R1 = 10 Ω
R2 = 100 Ω
R3 = 1 kΩ
R4 = 10 kΩ
R5 = 5 kΩ
R6 = 5 kΩ
R7 = 3 kΩ
POT1 = 10 Ω
POT2 = 100 Ω
POT3 = 1 kΩ
POT4 = 10 kΩ

Figure 2

3.3 DESIGN ANALYSIS

On top of our circuit design shown above, we have chosen an FDRM-K64F microprocessor that includes two on-chip ADCs each with 24 single-ended inputs or 8 differential inputs. As our input to the ADC becomes more complex, so do our testing considerations. In order for the ADC and microcontroller to use the measurements, we must ensure that their inputs have the required capacitance, resistance, and linearity.

4 Testing/Development

4.1 INTERFACE SPECIFICATIONS

Our final designs to be sent to our client's manufacturing plant must be completed using CADSTAR software.

4.2 HARDWARE/SOFTWARE

We have simulated our circuit using PSPICE to get an idea of the anticipated behavior of our circuit.

Going forward, we hope to build a current mirror circuit with two attenuating circuits on a breadboard in order to conduct physical experiments.

Throughout the testing phase, we will be watching three major results:

- Input current matches output current

- ADC input capacitance does not exceed 5 pF

- ADC input voltage is linearly proportional to actual voltage readings at critical current mirror nodes

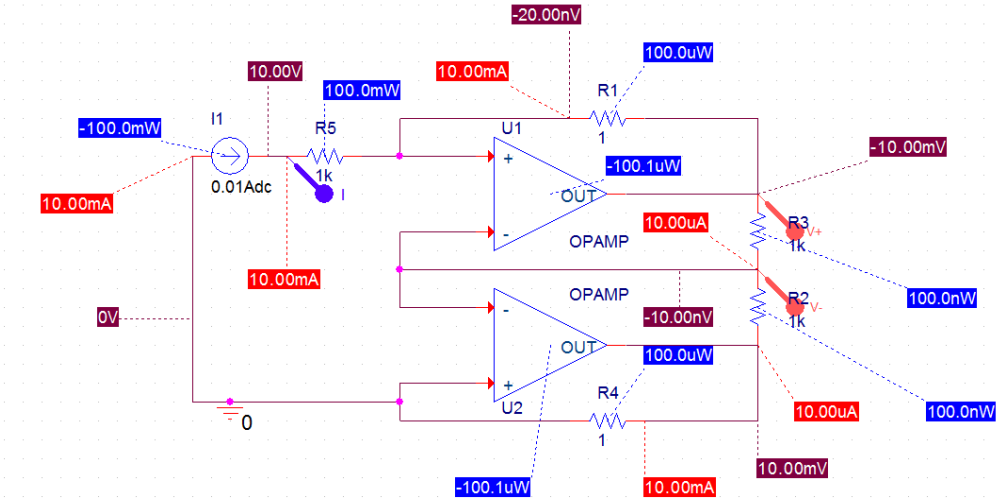
It is worth noting that at our current stage of the testing phase, we are primarily concerned with and capable of testing the first of the three listed results.

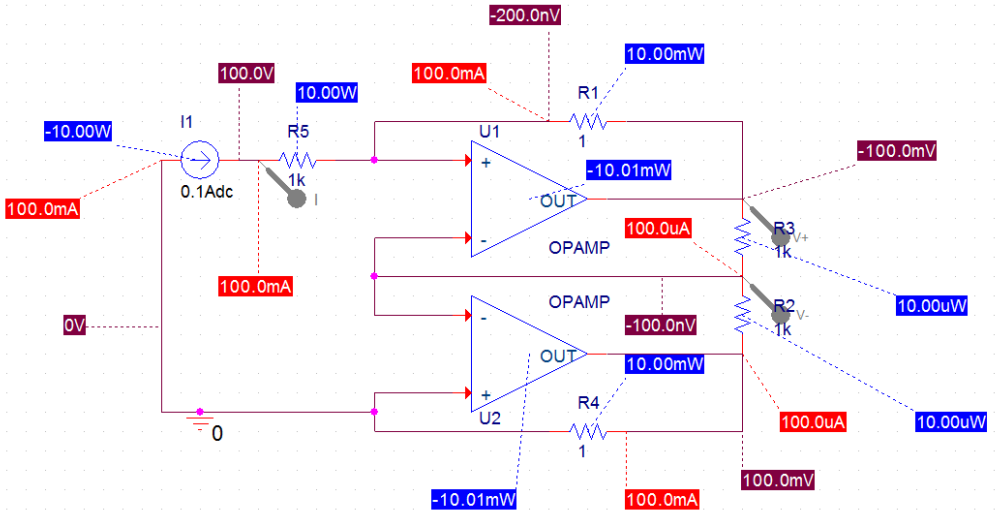
4.2 PROCESS

As we increase the number of components and complexity of the circuit, we must constantly check that the input and output currents remain equivalent. We are measuring two key voltages to obtain current and ultimately power. Doing so without disrupting the current of the circuit being measured is of the utmost importance.

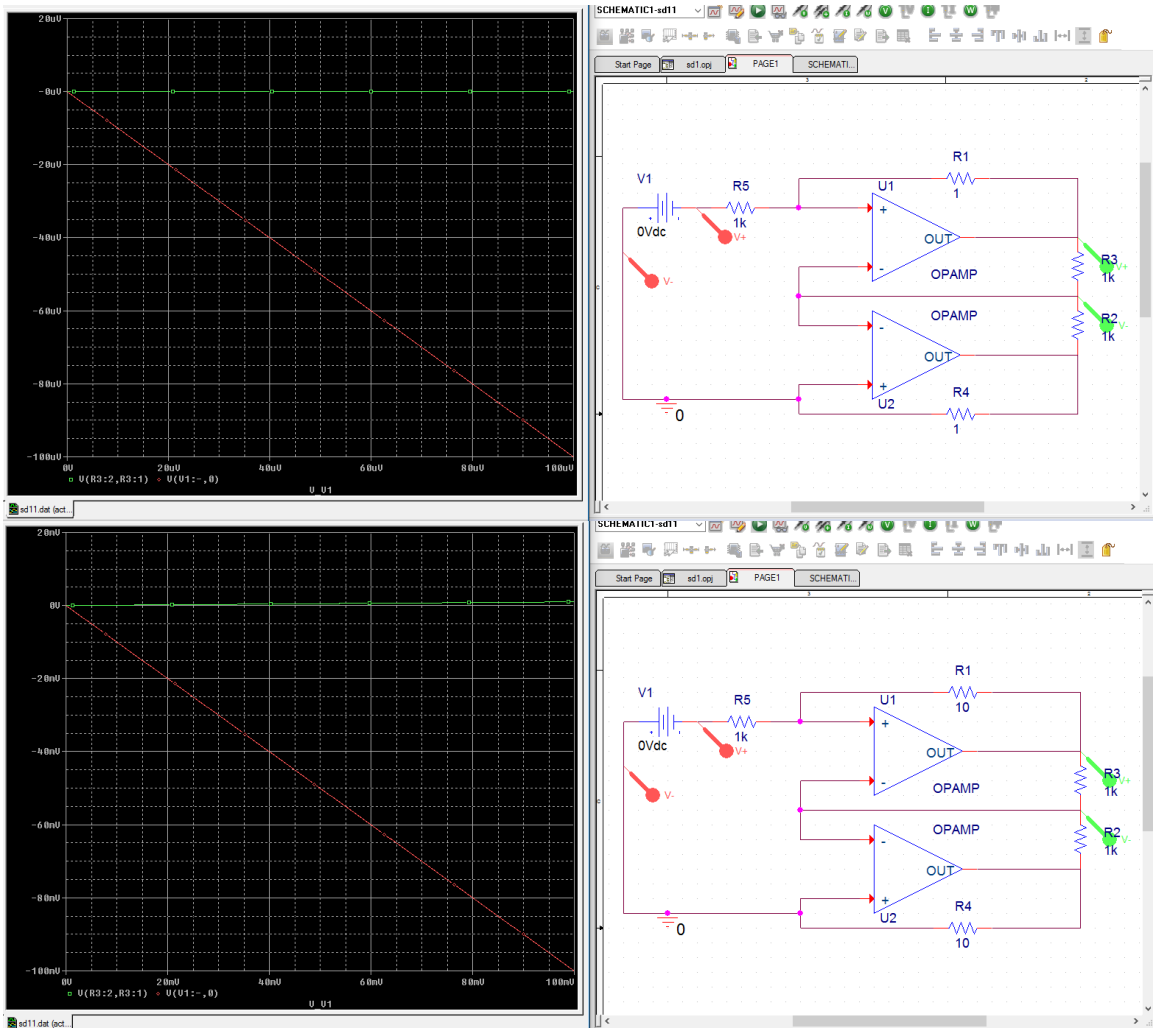
5 Results

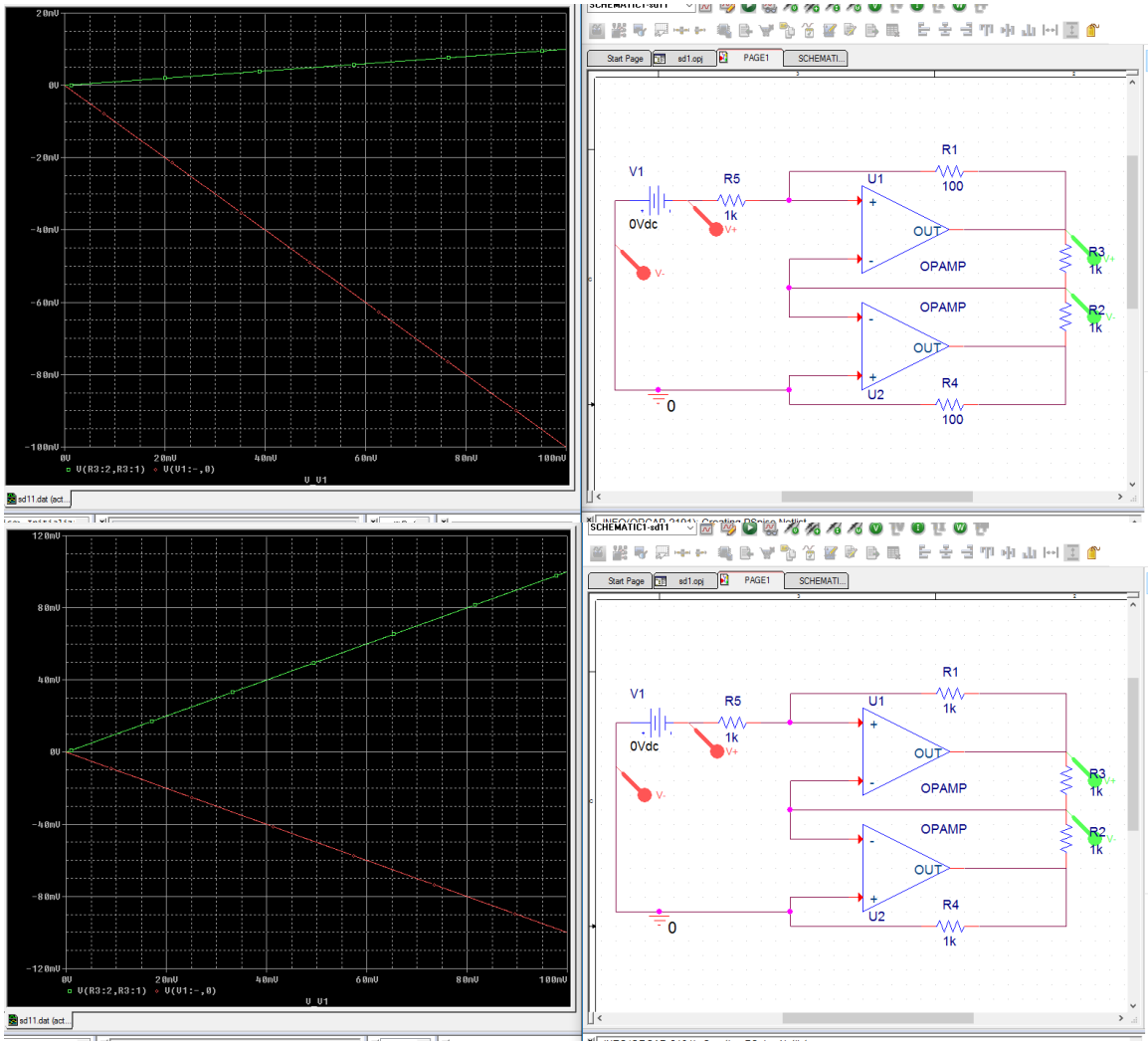
Below we simulated our current mirror circuit with two different input currents. We were pleased to see that the output current matched the input current in both cases – as expected.



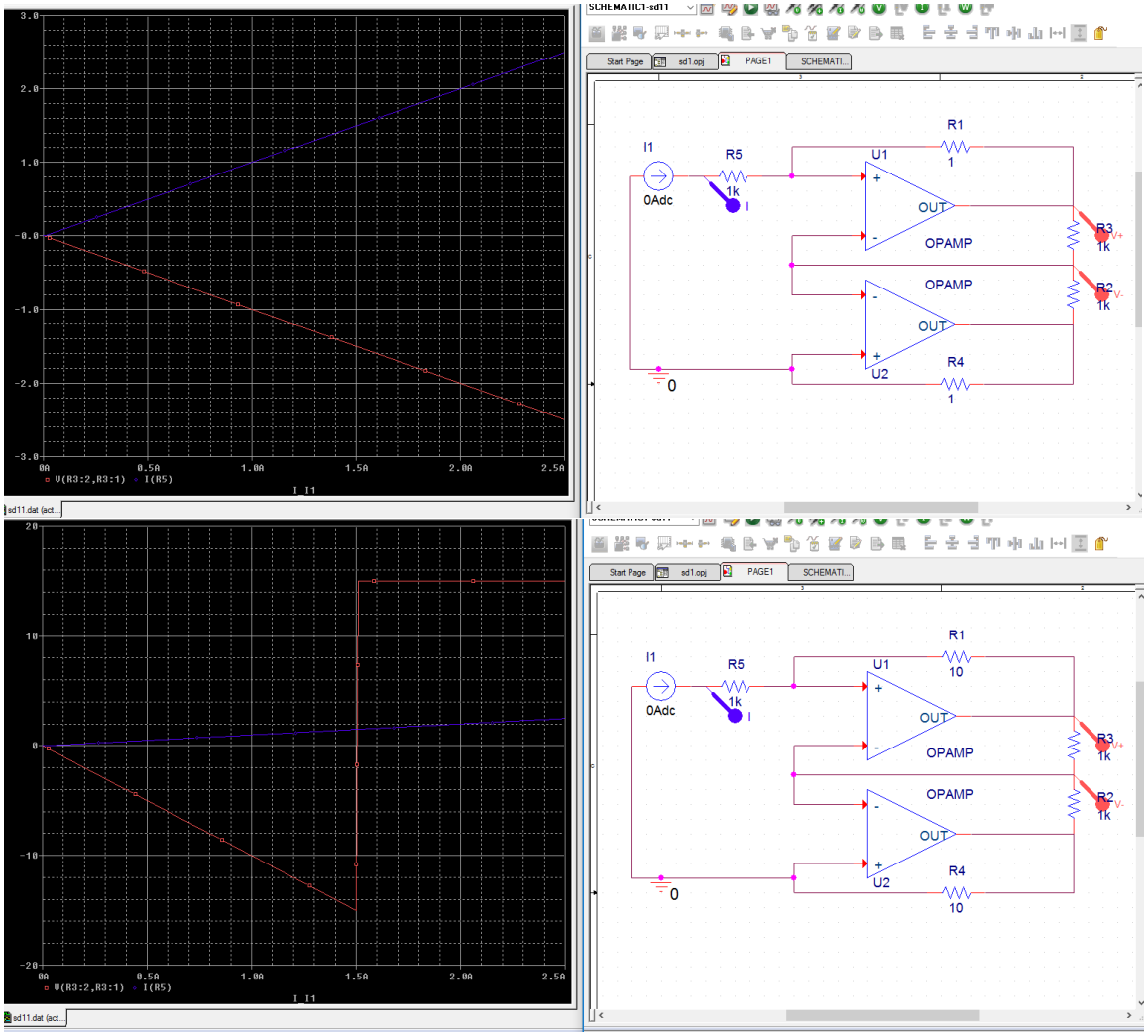


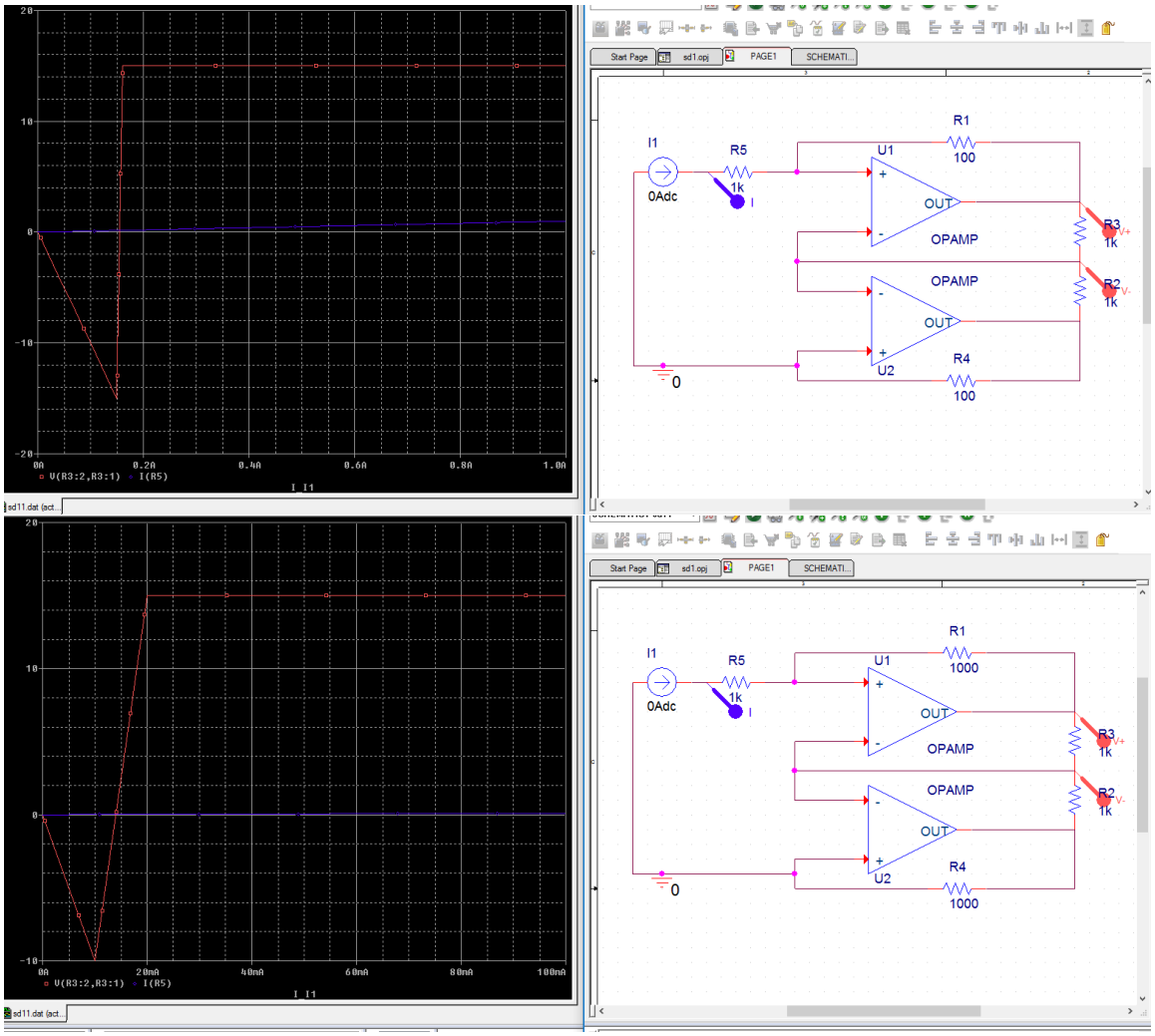
The four screenshots below show the results of a current mirror circuit simulation. We consider the circuit's behavior with a sweep of values for the voltage source. Each screenshot shows the behavior for a different range. The ranges are controlled by the positive feedback resistors.




20mV
0V
-20mV
-40mV
-60mV
-80mV
-100mV
0V
20mV
40mV
60mV
80mV
100mV
V(R3:2,R3:1) - V(V1:-,0)
V_V1
sd11.dat (act...
Start Page
sd1.opj
PAGE1
SCHEMATI...
V1
0Vdc
R5
1k
V+
V-
U1
OUT
OPAMP
R1
100
R3
1k
R2
1k
U2
R4
100
0
120mV
80mV
40mV
0V
-40mV
-80mV
-120mV
SCHEMATIC1-sd11

The four screenshots below represent the same ranges, but we know concern ourselves with a sweep of values for the input current.




20
10
0
-10
-20
0A
0.2A
0.4A
0.6A
0.8A
1.0A
V(R3:2,R3:1)
I(R5)
I_I1
sd11.dat (act...
Start Page
sd1.opj
PAGE1
SCHEMATI...
I1
0Adc
R5
1k
U1
R1
100
OUT
OPAMP
R3
1k
V+
R2
1k
V-
U2
R4
100
0
20
10
0
-10
0A
20mA
40mA
60mA
80mA
100mA
1000

6 Conclusions

During preliminary tests, our circuit behaved as expected. Going forward, we will add more circuit components in our software simulations, and we will build a physical breadboard test circuit. This next phase will include purchasing high-accuracy resistors and highly ideal operational amplifiers.

7 References

Not necessary for Version 1.

8 Appendices

Not necessary for Version 1.